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October 26, 2001

Attorney Docket No.: 08305-087002

Box Patent Application
Commissioner for Patents
Washington, DC 20231

Presented for filing is a new patent application claiming priority from a provisional patent application of:

Applicant: ALEXANDER I. KRYMSKI AND VLADIMIR BEREZIN

Title: FRAME SHUTTER FOR CMOS APS

Enclosed are the following papers, including those required to receive a filing date under 37 CFR §1.53(b):

	Pages
Specification	6
Claims	3
Abstract	1
Declaration	2
Drawing(s)	2

Enclosures:

— Assignment cover sheet and an assignment, 1 pages, and a separate $40 fee.
— Postcard.

Under 35 USC §119(e)(1), this application claims the benefit of prior U.S. provisional application 60/243,899, filed October 26, 2000.

CERTIFICATE OF MAILING BY EXPRESS MAIL

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10/26/2001
Date of Deposit

M.E. Augustine
Signature

Michael E. Augustine, Sr.
Typed or Printed Name of Person Signing Certificate

Basic filing fee	$740
Total claims in excess of 20 times $18	$0
Independent claims in excess of 3 times $84	$0
Fee for multiple dependent claims	$0
Total filing fee:	$740

A check for the filing fee is enclosed. Please apply any other required fees or any credits to deposit account 06-1050, referencing the attorney docket number shown above.

If this application is found to be incomplete, or if a telephone conference would otherwise be helpful, please call the undersigned at (858) 678-5070.

Kindly acknowledge receipt of this application by returning the enclosed postcard.

Please send all correspondence to:

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Respectfully submitted,

FOR Scott C. Harris
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Enclosures
SCH/dks
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Attorney's Docket No.: 08305-087002 / 08305-087P01

APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: FRAME SHUTTER FOR CMOS APS

APPLICANT: ALEXANDER I. KRYMSKI AND VLADIMIR BEREZIN

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Michael E. Augustine, Sr.
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FRAME SHUTTER FOR CMOS APS

CROSS-REFERENCE TO RELATED APPLICATIONS

This invention claims priority under 35 U.S.C. 119/120 from provisional application serial number 60/243,899 filed October 26, 2000.

TECHNICAL FIELD

This invention relates to complementary metal oxide semiconductor (CMOS) Active Pixel Sensors (APS), and more particularly to an improved frame-shutter for a CMOS APS.

BACKGROUND

CMOS active pixel image sensors may be operated using a "rolling" shutter. Such a shutter operates by reading out each row of pixels, and then resetting that individual row, and then rolling to read and then reset the next row of pixels. Each pixel hence gets read and then reset at slightly different times. Hence, each pixel has a slightly different time of integration. Some applications, such as high-speed photography, may require more time consistency than is possible using this approach. Therefore, in these other applications, a frame shutter may be used. In the frame shutter mode, all pixels in the array have substantially identical integration start times and integration stop times.

A typical CMOS Active Pixel Sensor (APS) 100 architecture utilizing a frame shutter is shown in Figure 1. The APS 100 includes a photoreceptor 105, a frame shutter 110, and an active pixel readout 115. The photoreceptor 105 may comprise, for example, a photogate or a photodiode. The frame shutter 110 includes sample and hold circuits as well as reset circuits. The sample and hold and reset circuits may be implemented using transistors. Figure 2 illustrates an APS 200 using a photogate 205 as the photoreceptor 105 and a PMOS frame shutter in a N-well 207. The PMOS frame shutter 207 includes PMOS transistors for the sample and hold circuits 210 and reset circuits 215, 220. The N-well pocket has a $+V_{dd}$ potential and insulates floating diffusion from photo=generated electrons. An active pixel readout 230 includes a source follower and row select circuits. The APS 200 architecture may reduce photo-generated charge cross-talk and increase the shutter efficiency. However, a photogate 205 as a photoreceptor has a low quantum efficiency and a relatively large dark current. Also, the N-well insert in the pixel significantly reduces the fill factor and increases the minimum pixel pitch.

SUMMARY

A CMOS Active Pixel Sensor (APS) uses a pinned photodiode as a photoreceptor and negative-channel metal-oxide semiconductor (NMOS) transistors in the sample and hold and reset circuits of the frame shutter. The pinned photodiode increases the quantum efficiency and reduces the dark current. The NMOS transistors in the frame shutter increases the fill factor and reduces the pixel pitch.

DESCRIPTION OF DRAWINGS

These and other features and advantages of the invention will become more apparent upon reading the following detailed description and upon reference to the accompanying drawings.

Figure 1 illustrates a typical CMOS Active Pixel Sensor (APS) architecture utilizing a frame shutter.

Figure 2 illustrates an APS using a photogate as the photoreceptor and PMOS transistors for the sample and hold circuits and reset circuits.

Figure 3 illustrates an APS using a pinned photodiode as the photoreceptor.

Figure 4 illustrates an APS using a photogate as the photoreceptor and NMOS transistors for the sample and hold circuits and reset circuits.

Figure 5 illustrates an APS using a pinned photodiode as the photoreceptor and PMOS transistors for the sample and hold circuits and reset circuits.

DETAILED DESCRIPTION

CMOS APS for high-speed machine imaging needs freeze-frame simultaneous electronic shutter. Although the previous architectures reduced the photo-generated cross-talk and increased shutter efficiency, there is still a need to improve the quantum efficiency and decrease the dark current, as well as increasing the fill factor and reducing the pixel pitch.

Figure 3 illustrates an APS 300 using a pinned photodiode 305 as the photoreceptor 105 according to one embodiment of the invention. Pinned photodiodes have been employed within charge coupled devices and have shown advantages in the area of color response for blue light, dark current density and image lag. Thus, using a pinned photodiode 305 as the photoreceptor should increase the quantum efficiency and decrease the dark current. The APS 300 includes the pinned photodiode 305 connected to a PMOS Frame Shutter 310 in a N-well, as well as an active pixel readout circuit 320. This embodiment may be used when quantum efficiency and dark current are concerns.

A second embodiment of the present invention may be used when fill factor and pixel pitch are the primary concerns. Figure 4 illustrates an APS architecture 400 using a photogate or photodiode as the photoreceptor 105 and NMOS transistors for the sample and hold circuits and reset circuits. A The frame shutter 405 is a NMOS frame shutter in a P-well. NMOS transistors are used for the sample and hold circuits 410 and the reset circuits 415, 420. The N-well insert in a pixel significantly reduces the fill factor and increases the minimum pixel pitch. By replacing the N-well with the P-well, the fill factor is increased and the pixel pitch reduced. An active pixel readout circuit 430 is connected to the frame shutter 405.

A third embodiment of the present invention combines the use of a pinned photodiode as the photoreceptor and the use of NMOS transistors for the sample and hold circuits and reset circuits. Figure 5 illustrates an APS architecture 500 using a pinned photodiode 305 as the photoreceptor 105 and PMOS transistors for the sample and hold circuits and reset circuits. In this embodiment, the pinned photodiode 305 is connected to the NMOS Frame Shutter 405 in a P-well, as well as an active pixel readout circuit 530. The NMOS transistors are used for the sample and hold circuits 410 and the reset circuits 415, 420. The pinned photodiode 305 as the

photoreceptor increases the quantum efficiency and decreases the dark current, while the P-well increases the fill factor and reduces the pixel pitch.

Numerous variations and modifications of the invention will become readily apparent to those skilled in the art. Accordingly, the invention may be embodied in other specific forms without departing from its spirit or essential characteristics.

WHAT IS CLAIMED IS:

1. An active pixel sensor comprising:

a photoreceptor, wherein the photoreceptor comprises a pinned photodiode;

a frame shutter; and

an active pixel readout.

2. The active pixel sensor of Claim 1, wherein the frame shutter is a PMOS frame shutter in a N-well.

3. The active pixel sensor of Claim 2, wherein the frame shutter includes sample and hold and reset circuits.

4. The active pixel sensor of Claim 3, wherein the sample and hold and reset circuits comprise PMOS transistors.

5. The active pixel sensor of Claim 1, wherein the pinned photodiode increases the quantum efficiency.

6. The active pixel sensor of Claim 1, wherein the pinned photodiode reduces dark current.

7. An active pixel sensor comprising:

a photoreceptor;

a frame shutter, wherein the frame shutter is a PMOS frame shutter in a N-well; and

an active pixel readout.

8. The active pixel sensor of Claim 7, wherein the photoreceptor comprises a photodiode or a photogate.

9. The active pixel sensor of Claim 7, wherein the frame shutter includes sample and hold and reset circuits.

10. The active pixel sensor of Claim 9, wherein the sample and hold and reset circuits comprise NMOS transistors.

11. The active pixel sensor of Claim 7, wherein the PMOS frame shutter increases the fill factor.

12. The active pixel sensor of Claim 7, wherein the PMOS frame shutter reduces the pixel pitch.

13. An active pixel sensor comprising:

a photoreceptor, wherein the photoreceptor comprises a pinned photodiode;

a frame shutter, wherein the frame shutter comprises a NMOS frame shutter in a P-well; and

an active pixel readout.

14. The active pixel sensor of Claim 13, wherein the frame shutter includes sample and hold and reset circuits.

15. The active pixel sensor of Claim 14, wherein the sample and hold and reset circuits comprise NMOS transistors.

16. The active pixel sensor of Claim 13, wherein the pinned photodiode increases the quantum efficiency.

17. The active pixel sensor of Claim 13, wherein the pinned photodiode reduces dark current.

18. The active pixel sensor of Claim 13, wherein the PMOS frame shutter increases the fill factor.

19. The active pixel sensor of Claim 13, wherein the PMOS frame shutter reduces the pixel pitch.

ABSTRACT

A CMOS Active Pixel Sensor (APS) uses a pinned photodiode as a photoreceptor and negative-channel metal-oxide semiconductor (NMOS) transistors in the sample and hold and reset circuits of the frame shutter. The pinned photodiode increases the quantum efficiency and reduces the dark current. The NMOS transistors in the frame shutter increase the fill factor and reduce the pixel pitch.

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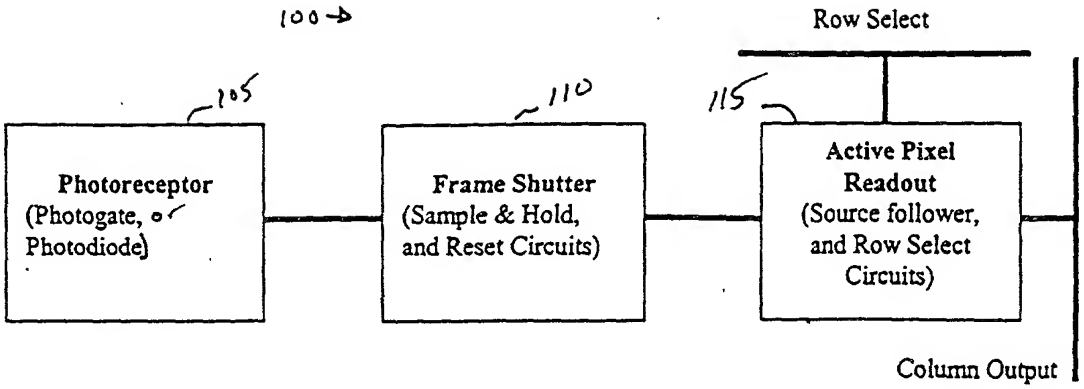

Figure 1

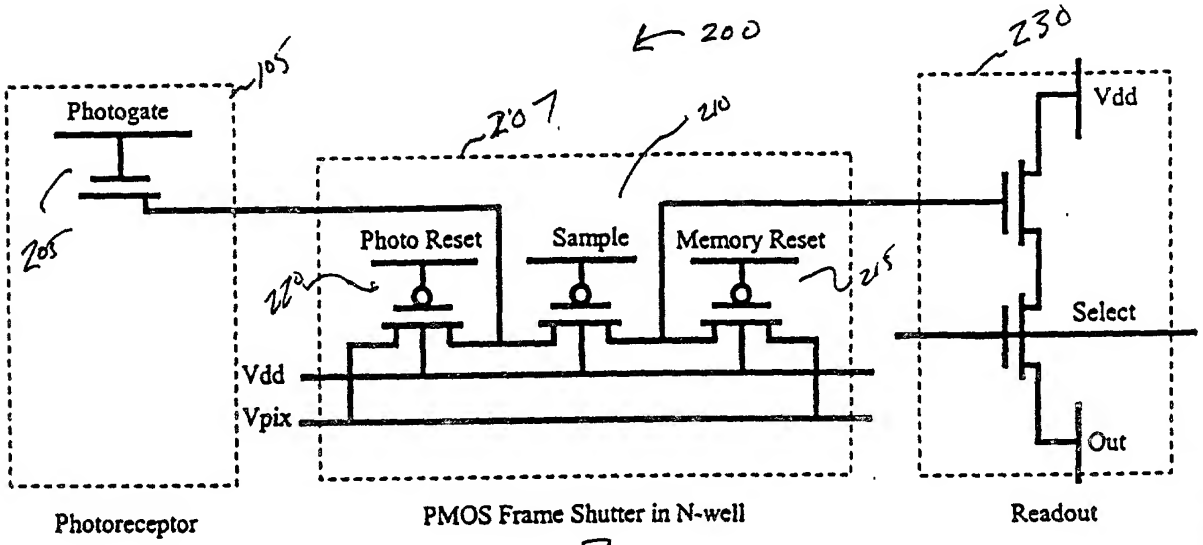

Figure 2

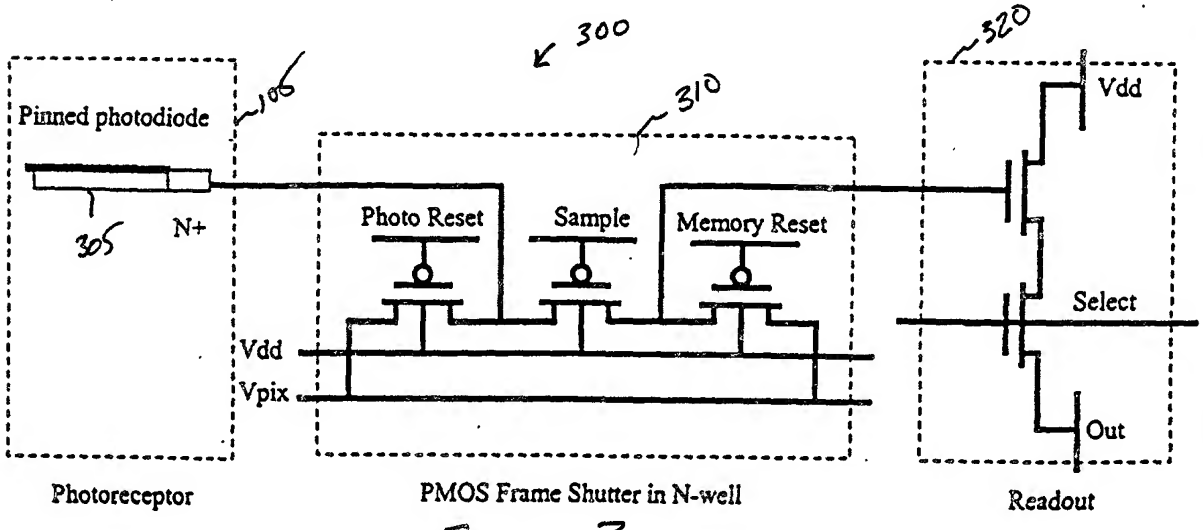

Figure 3

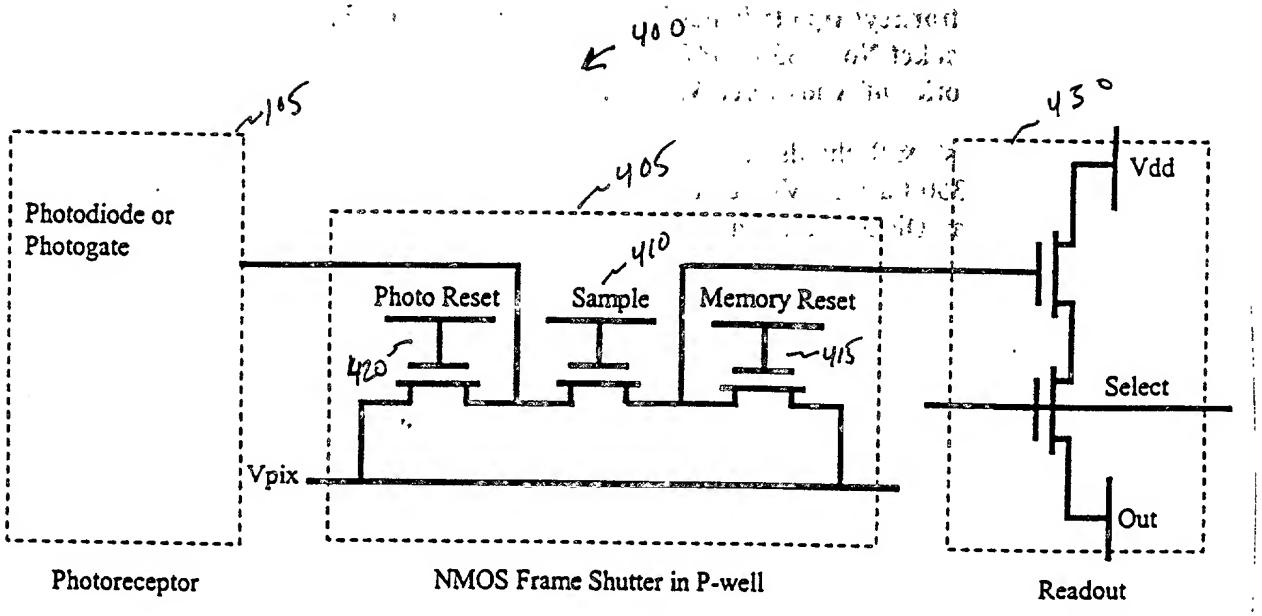

Figure 4

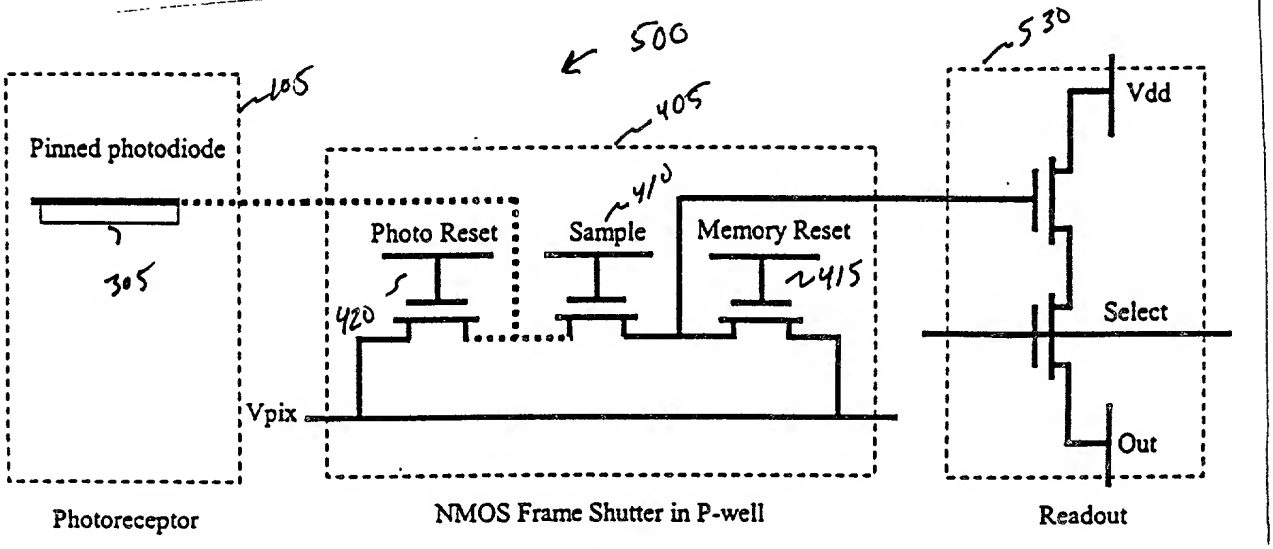

Figure 5

Attorney's Docket No.: 08305-087002

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled FRAME SHUTTER FOR CMOS APS, the specification of which:

[X] is attached hereto.

[] was filed on _____ as Application Serial No. _____ and was amended on _____.

[] was described and claimed in PCT International Application No. _____ filed on _____ and as amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information I know to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim the benefit under Title 35, United States Code, §119(e)(1) of any United States provisional application(s) listed below:

U.S. Serial No.	Filing Date	Status
60/243,899	October 26, 2000	Pending

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose all information I know to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

U.S. Serial No.	Filing Date	Status

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

Country	Application No.	Filing Date	Priority Claimed

I hereby appoint the following attorneys and/or agents to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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Attorney's Docket No.: 08305-087002
Client's Ref. No.: 08305-087P01

Combined Declaration and Power of Attorney

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patents issued thereon.

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